## Introduction

This evaluation board is designed to help the customer evaluate the 9FGV1006 device. When the board is connected to a PC running IDT Timing Commander ${ }^{\text {TM }}$ Software through USB, the device can be configured and programmed to generate different combinations of frequencies. This evaluation board is designed for differential outputs. It can not be used for single-ended outputs.

## Board Overview

Use Figure 1 and Table 1 to identify: power supply jacks, USB connector, input and output frequency SMA connectors.
Figure 1. Evaluation Board Overview


Table 1. Evaluation Board Pins and Functions

| Label Number | Name | On-board Connector Label | Function |
| :---: | :---: | :---: | :---: |
| 1 | $I^{2} \mathrm{C}$ interface Connector | J2 | Alternative $\mathrm{I}^{2} \mathrm{C}$ interface connector for Aardvark. IDT Timing Commander can also use Aardvark. |
| 2 | USB Connector | J6 | Connect this USB to your PC to run IDT Timing Commander. <br> The board can be powered from the USB port. |
| 3 | Output Power Supply Jack | J3 | Connect to $1.8 \mathrm{~V}, 2.5 \mathrm{~V}$ or 3.3 V for the output voltage of the device. |
| 4 | Core Power Supply Jack | J4 | Connect to $1.8 \mathrm{~V}, 2.5 \mathrm{~V}$ or 3.3 V for the core voltage of the device. |
| 5 | Ground Jack | J5 | Connect to ground of power supply. |
| 6 | Differential Output 1 | S3 \& S4 | This can be a differential pair, or two single-ended outputs. <br> Available logic types: LVCMOS, LVDS and LP-HCSL. |
| 7 | Differential Output 2 | S7 \& S10 | This can be a differential pair, or two single-ended outputs. <br> Available logic types: LVCMOS, LVDS and LP-HCSL. |
| 8 | Power Supply Voltage Selector | E1, E2, E3 | VDD_REFP1, VDDO_0, VDDO_1, four-way headers used to select a power supply voltage. Connect the center pin to one of the 4 surrounding pins to select a voltage or a source. |
| 9 | Power Supply Voltage Selector | E4 | VDDA0, four-way headers used to select a power supply voltage. Connect the center pin to one of the 4 surrounding pins to select a voltage or a source. |
| 10 | Reference Output 0 | S1 | Reference or buffered output from the crystal. |
| 11 | Sel_I2C\# | JP3 | $1^{2} \mathrm{C}$ bus enable access registers. OTP bank CFG0 used to initialize RAM configuration registers. |
| 12 | SCL, SDA / SEL0, SEL1 | JP1, JP2 | OTP bank CFG used to initialize RAM configuration registers. |

## Board Power Supply

The evaluation board uses jumpers E1-E4 to set the power supply voltages for various $V_{D D}$ pins. The 4 -way jumpers can select 3 different voltages from regulators that use power from the USB port. Selection \#2 is the jack for connecting a bench power supply.

E1: Power supply for the REF outputs. The E1 voltage also determines the LVCMOS output levels of the REF0 and REF1 outputs.
E2: Power supply for the OUTO output driver.
E3: Power supply for the OUT1 output driver.
E4: Power supply for the analog $\left(\mathrm{V}_{\mathrm{DDA}}\right)$ and digital $\left(\mathrm{V}_{\mathrm{DDD}}\right)$ core $\mathrm{V}_{\mathrm{DD}}$ pins.
See the 9FGV1006 PCle Evaluation Board Schematics (Figure 4-Figure 7) for detailed information.

## Interfacing with a Computer to Run Timing Commander

As shown in Figure 2, jumpers JP1 and JP2 are installed to use the FTDI chip U6 for connecting to the computer with the USB port J6.
The U6 chip translates USB to $I^{2} \mathrm{C}$.
When using Aardvark, remove jumpers JP1 and JP2 and connect the Aardvark to connector J2. Default $\mathrm{I}^{2} \mathrm{C}$ device address for the 9FGV1006 is $0 \times 68$.

Miscellaneous interfaces can connect to J2 pin 1 for the Serial Clock and to J2 pin 3 for the Serial Data signal. J2 pin 2 can be used as ground, but any other ground pin will also work.

When OTP in the 9FGV1006 device is burned with multiple configurations, JP1 and JP2 can be applied in JP3 position respectively. Connect JP3 (SEL_I2C\#) to VDDO and power-up the 9FGV1006 in Hardware Select mode. This enables changing between 4 configurations with SELO/1.

Figure 2. Connecting to a Computer via USB Port J6


## On-board Crystal

A 25 MHz crystal is installed on the board and is used as the reference frequency. The board can also be modified to insert an external reference clock into the XIN pin using SMA connector S11. When using an external reference clock, additional components need to be assembled and the crystal needs to be removed.

## Output Terminations

Each differential output has a pair of SMA connectors to connect to a $50 \Omega$ coax. It is recommended to combine the two signals using a balun or splitter/combiner device when measuring jitter or phase noise. The circuit at the SMA connectors is shown in Figure 3.

Figure 3. SMA Connectors Circuit


The circuit is designed for maximum flexibility when testing all possible logic types. Default assembly uses a $0.1 \mu \mathrm{~F}$ capacitor in place of R14 and R16, and the short across R14 and R16 is cut. No other devices are assembled. This simple AC-coupled configuration allows for testing phase noise and jitter of all possible logic types. The circuit can be modified for custom tests. TP3 is a position to place a differential FET probe.

## Operating Instructions

1. Set all jumpers for power supply choices (E1-E6), interface choices (JP1 and JP2), and set the U2 switches.
2. Connect an interface: USB or $I^{2} \mathrm{C}$.
3. In the case of an $I^{2} \mathrm{C}$ interface, also connect external power supply to jacks J 3 , J 4 and J 5 .
4. Start Timing Commander for either USB or Aardvark.
a. Start new configuration or load TCS file for existing configuration.
b. Choose PhiClock personality.
c. For Aardvark, click to select Aardvark "Connection Interface".
d. For a new configuration, prepare all settings.
e. Click to connect to the 9FGV1006 device. Top right should turn green.
f. Click : to write all settings to the 9FGV1006 device.
g. It should now be possible to measure clocks on outputs.
h. While connected, each change to the settings will be written to the 9FGV1006 immediately and can be observed at the clock outputs.

## Schematics

Figure 4. 9FGV1006 PCIe Evaluation Board Schematic - page 1


Figure 5. 9FGV1006 PCle Evaluation Board Schematic - page 2


Figure 6. 9FGV1006 PCIe Evaluation Board Schematic - page 3


Figure 7. 9FGV1006 PCle Evaluation Board Schematic - page 4


## Ordering Information

| Orderable Part Number | Description |
| :---: | :---: |
| EVK9FGV1006 | Evaluation board with all differential outputs AC coupled. |

## Revision History

| Revision Date | Description of Change |
| :--- | :--- |
| May 17, 2018 | Updated evaluation board schematics. |
| February 28, 2018 | Updated numbering and labeling in Evaluation Board Pins and Functions table and Evaluation Board <br> Overview diagram. |
| November 27, 2017 | Initial release. |

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