

ISL21010XXEV1Z User's Guide

Introduction

The ISL21010XXEV1Z evaluation board is designed to measure the performance of the low dropout voltage ISL21010 voltage reference. The reference comes in a wide selection of output voltages ranging from 1.024V to 4.096V, and an initial accuracy of 0.2%. With a typical temperature coefficient of 15ppm/°C and 25mA output current source capability, the ISL21010 is ideal for general purpose industrial applications.

The evaluation board includes voltage input test points (VIN and GND) for a power supply input, as well as a pair of test points for the output (VOUT and GND). Additionally, a jumperable R-C damper network can be connected to VOUT (J1), and R2 accepts surface mount or through hole style resistors for the output load testing.

Reference Documents

• ISL21010 Datasheet, FN7896

TABLE 1. ORDERING INFORMATION

BOARD NUMBER	OUTPUT VOLTAGE (V)	TYPE
ISL2101010EV1Z	1.024	Evaluation Board
ISL2101012EV1Z	1.25	Evaluation Board
ISL2101015EV1Z	1.5	Evaluation Board
ISL2101020EV1Z	2.048	Evaluation Board
ISL2101025EV1Z	2.5	Evaluation Board
ISL2101030EV1Z	3.0	Evaluation Board
ISL2101033EV1Z	3.3	Evaluation Board
ISL2101041EV1Z	4.096	Evaluation Board

ISL21010XXEV1Z Board

The schematic of the evaluation board is shown in Figure 5. The ISL21010XXEV1Z contains the ISL21010 voltage reference (U1), the input decoupling capacitors (C1, C2), and a load capacitor (C3). The power supply leads attach to TP1 and TP2 (VIN, GND). The output is measured at test points TP3 and TP4 (VOUT, GND).

The R-C damper network is populated and can be connected to the reference output by adding a shunt to the R-C jumper (J1). The damper network improves stability by reducing transient load ringing with high value (>0.47 μ F) capacitors.

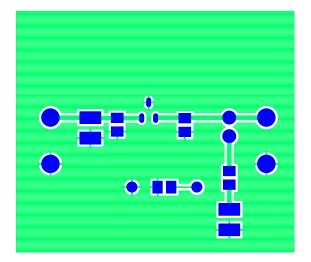
TABLE 2. COMPONENTS PARTS LIST

DEVICE #	VALUE	DESCRIPTION
C1	10µF	Bypass Capacitor
C2	0.1µF	Bypass Capacitor
C3	0.22μF	Load Capacitor
C4	10µF	Damper Capacitor
R1	2.21kΩ	Damper Resistor
R2	DNP	Optional Load Resistor
U1	ISL21010	SOT-23 3-Pin Package
J1	DNP	Damper Jumper



FIGURE 1. VOLTAGE REFERENCE EVALUATION BOARD

Voltage Reference Evaluation Board Layout



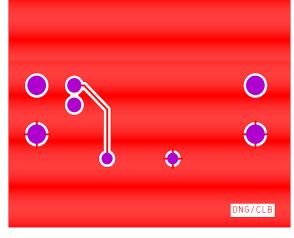


FIGURE 2. TOP COMPONENTS

FIGURE 3. BOTTOM LAYER

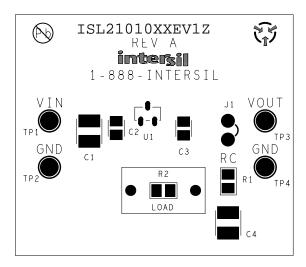


FIGURE 4. ASSEMBLY DRAWING

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.

GND

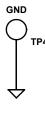


FIGURE 5. SCHEMATIC

VOUT